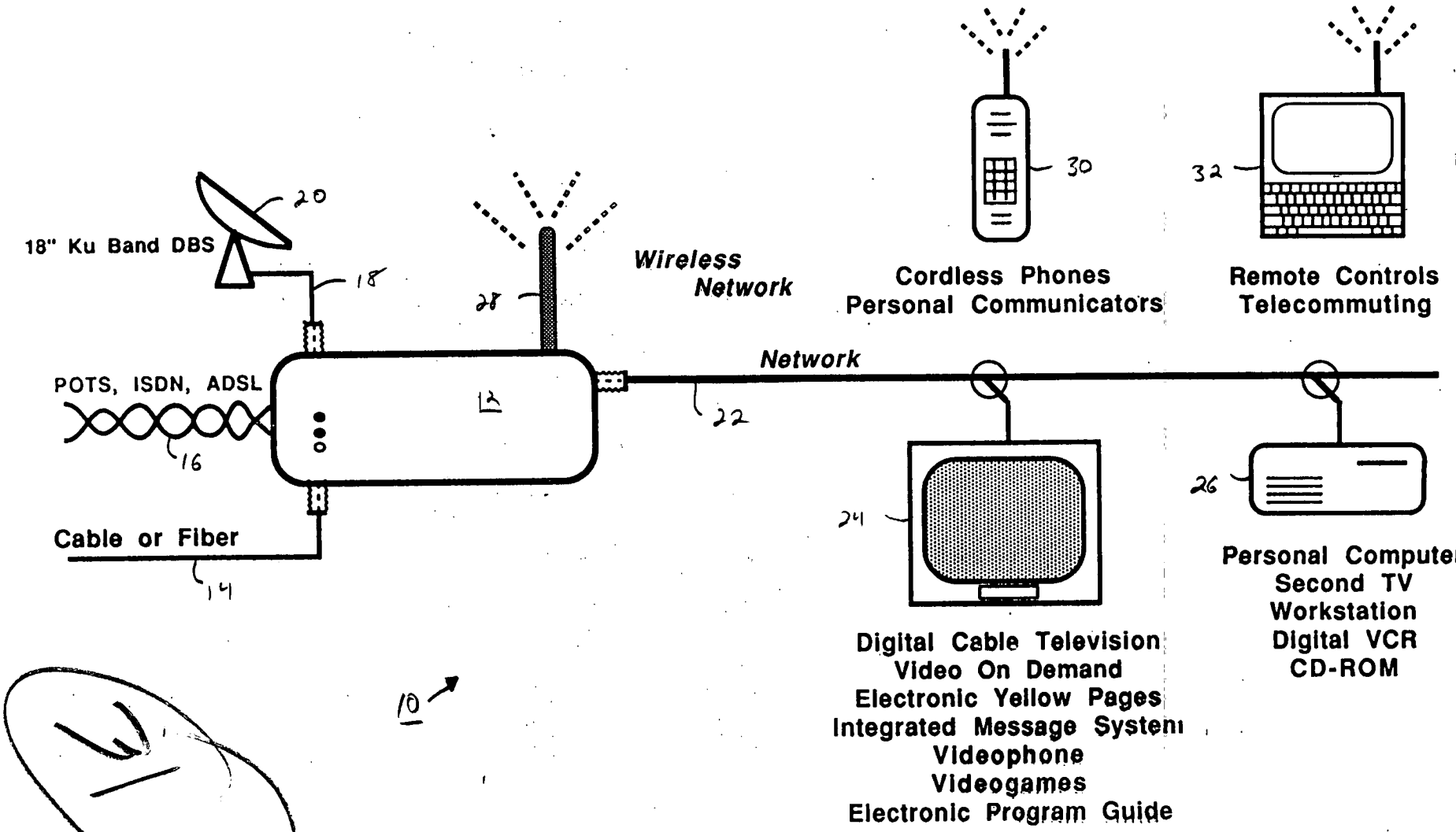
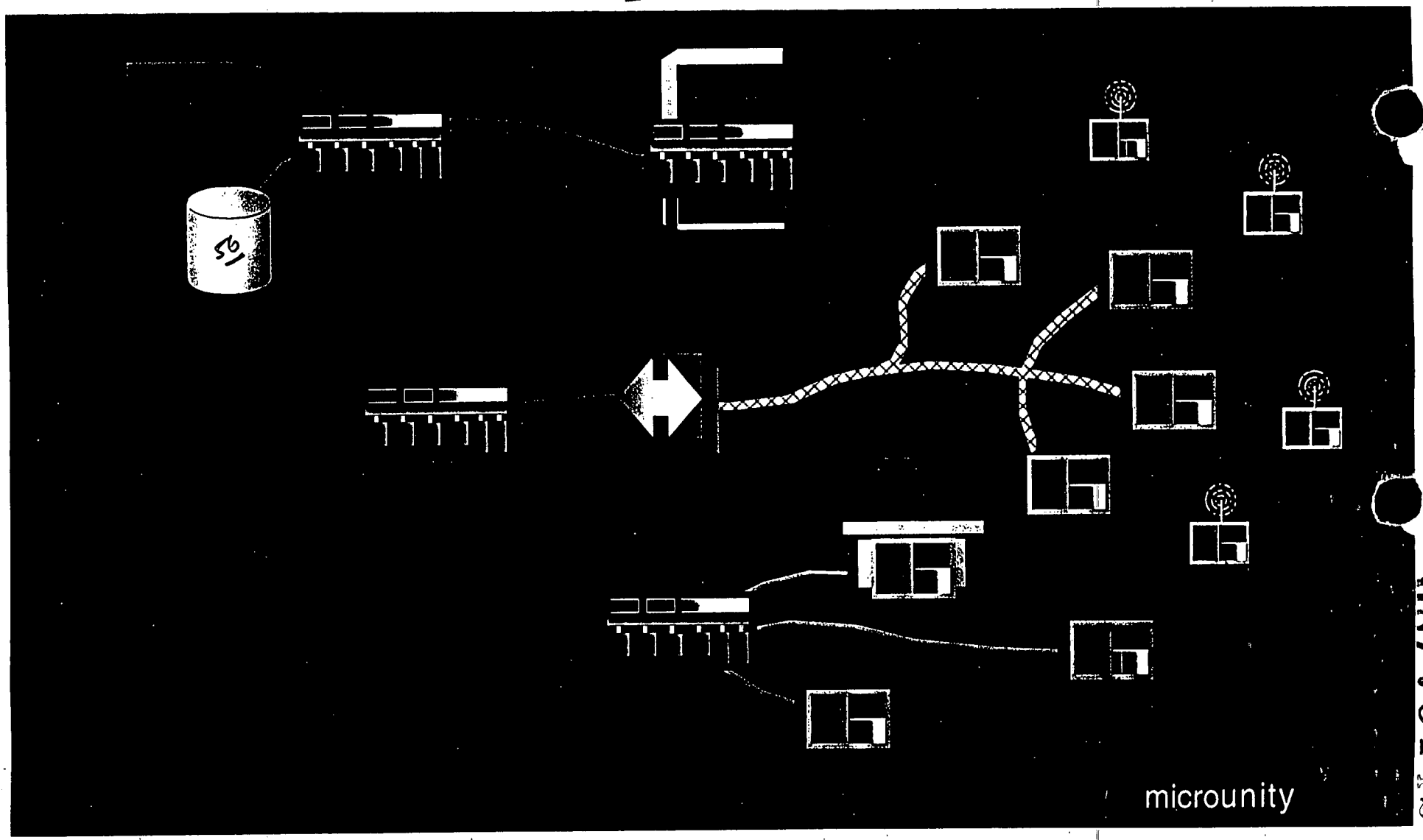


Figure 1

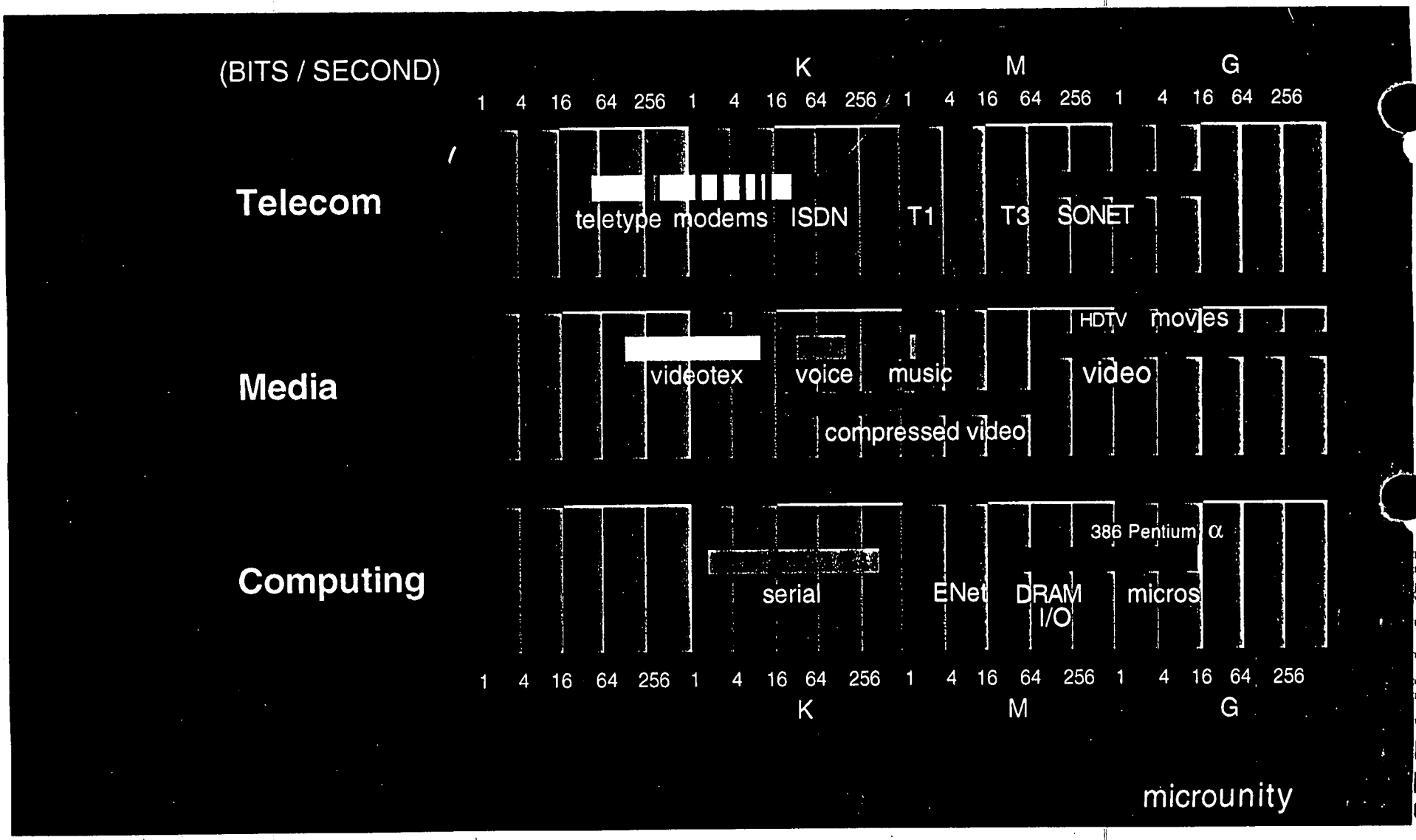
08/054,429

Figure 2



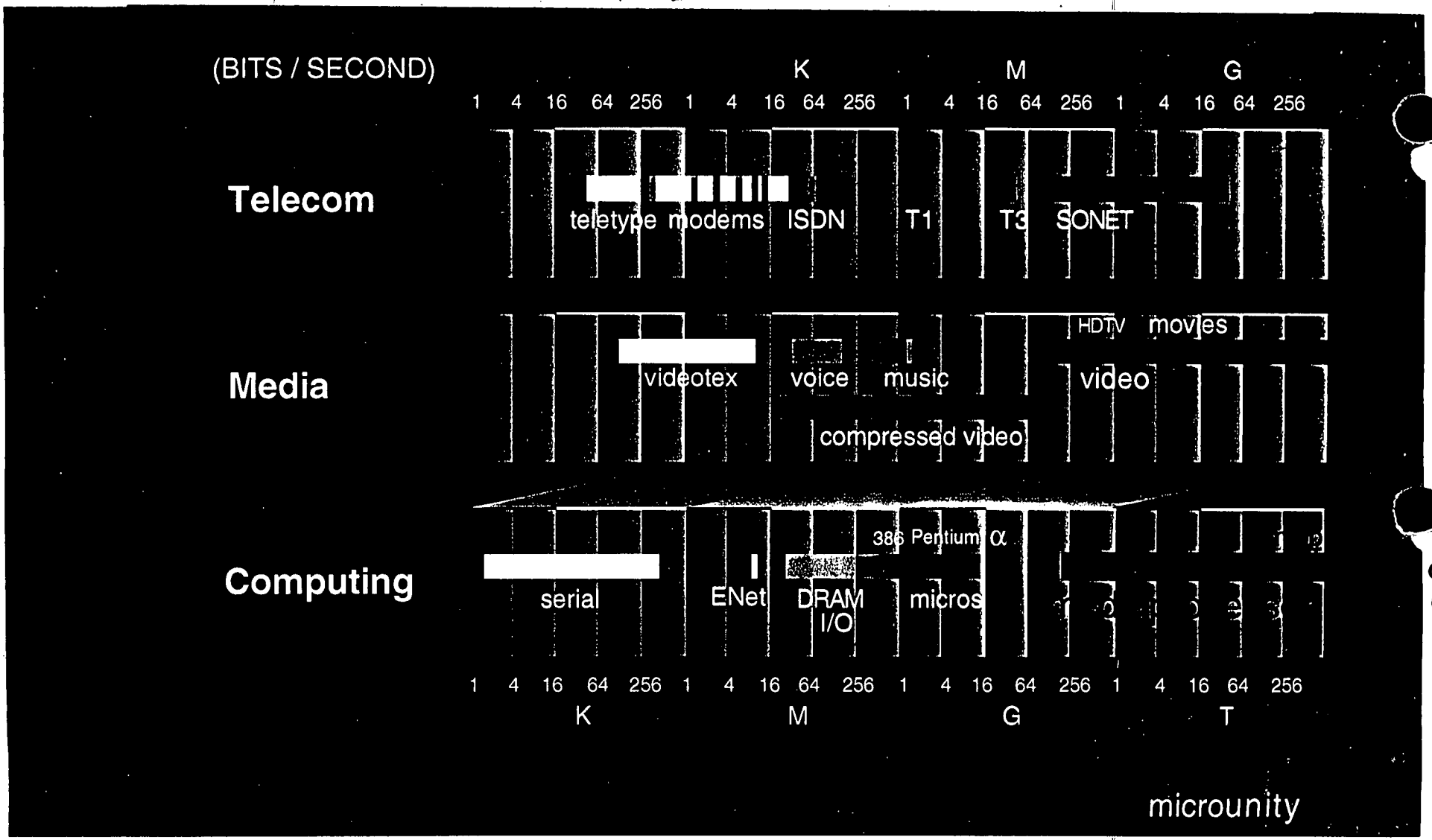
08/254,429

Figure 3



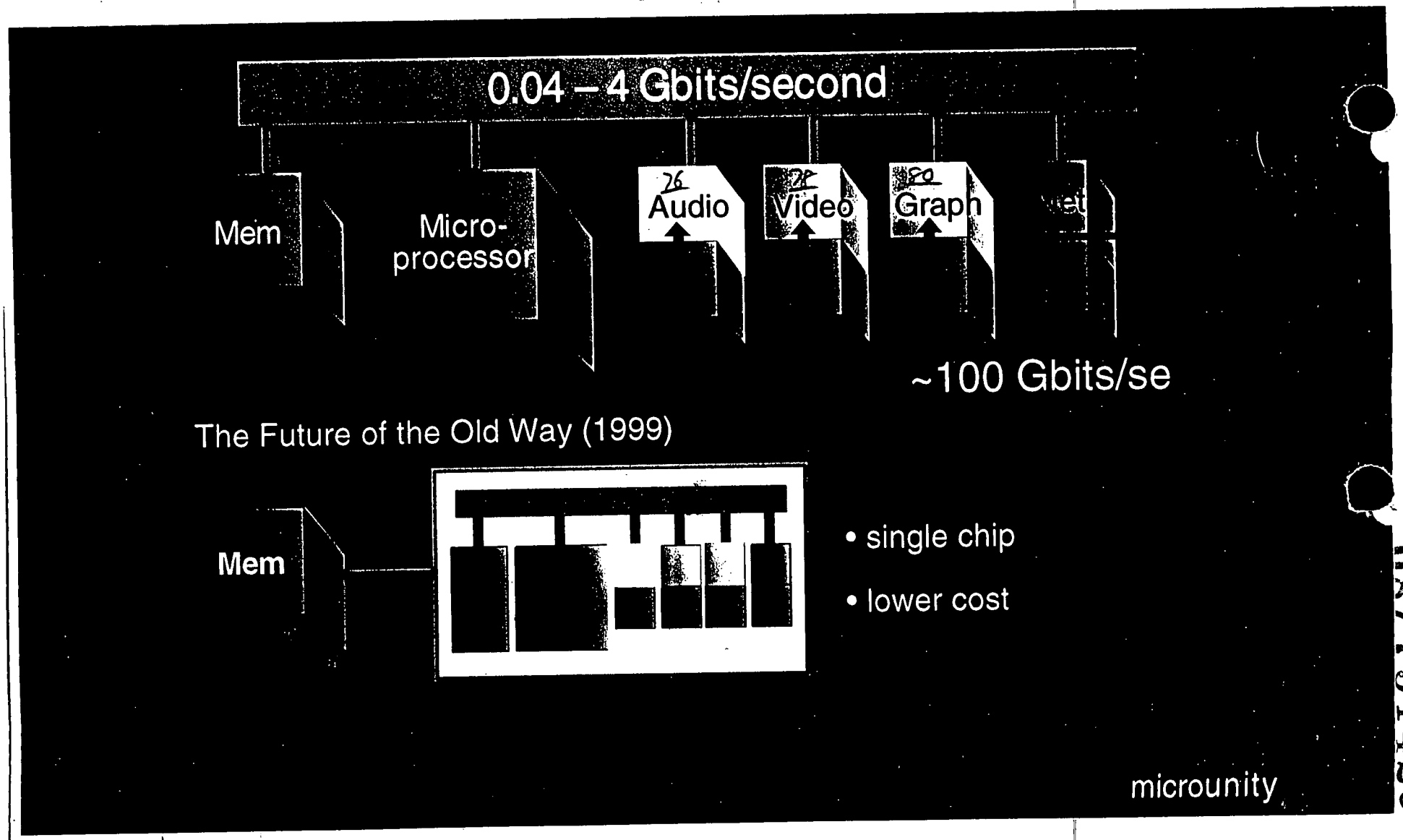
08754429

Figure 4



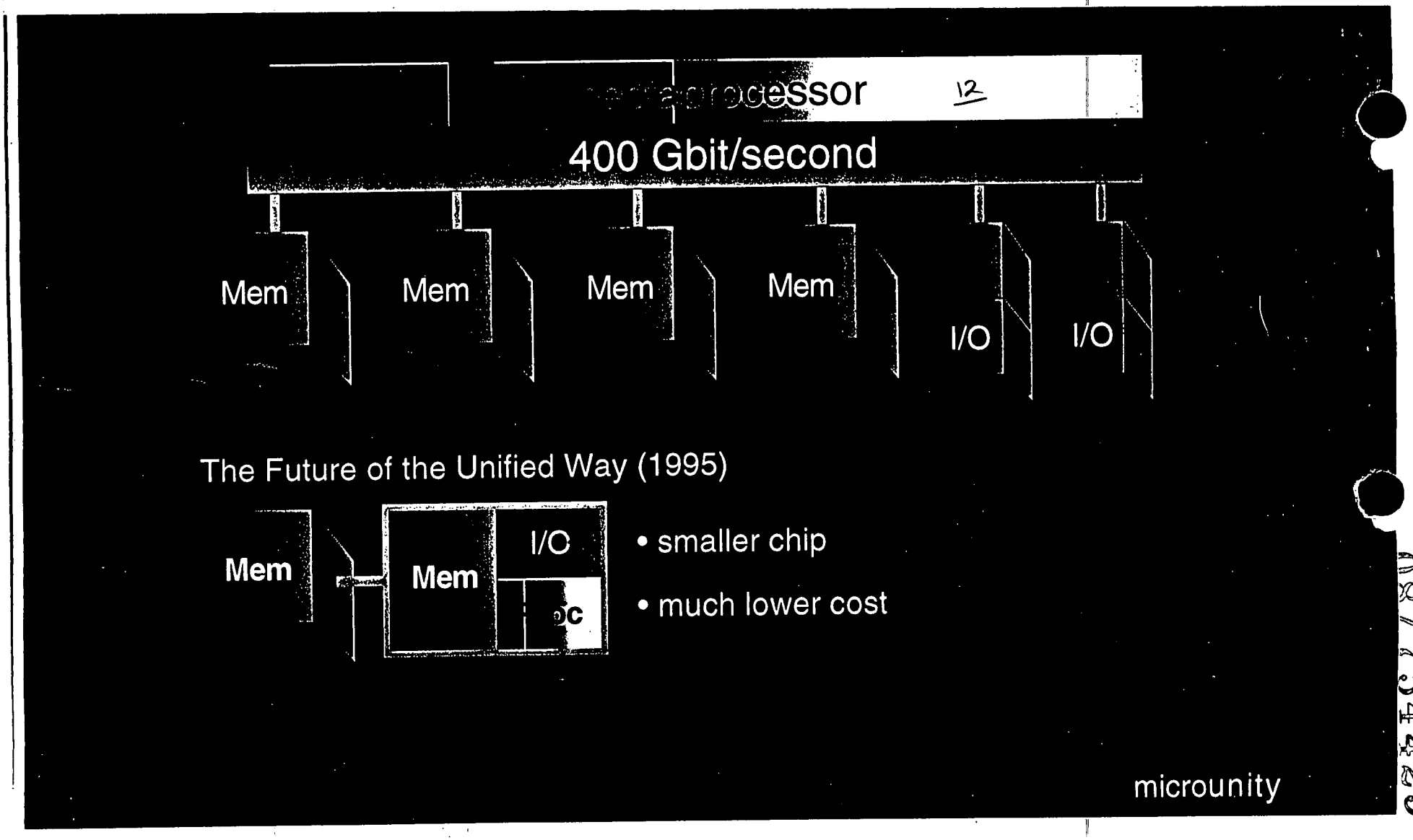
08/574,429

Figure 5



08/754,429

Figure 6



08/754,429

Figure 7

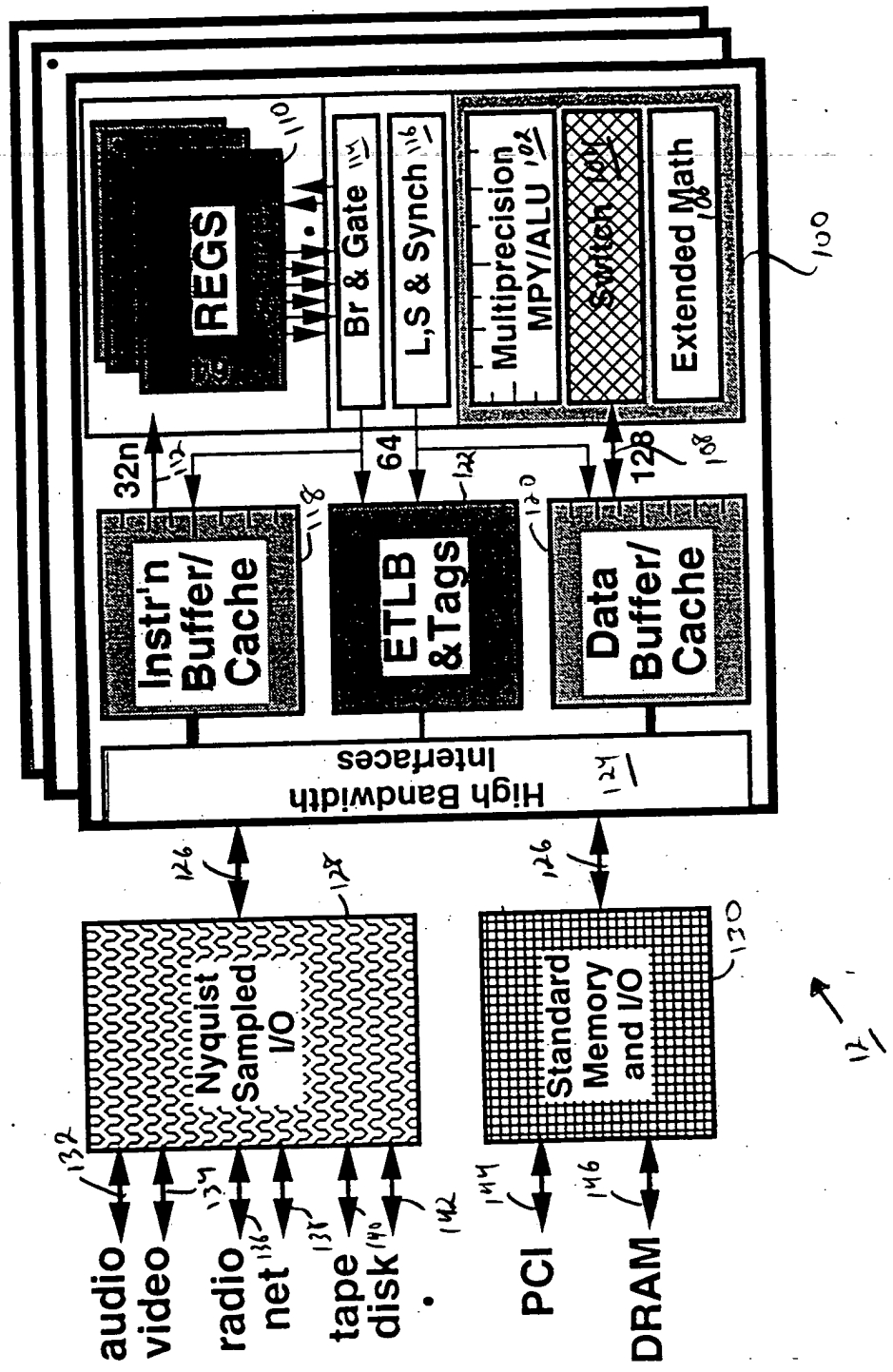
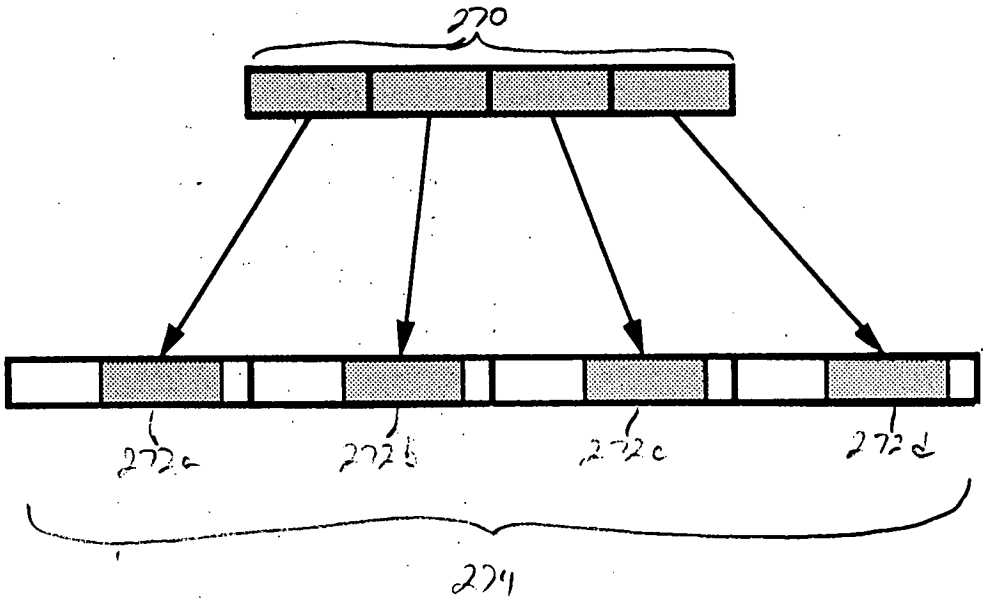

REGS
Br & Gate
L,S & Synch
Multiprecision MPY/ALU
Switch
Extended Math
100
110
32n
64
128
Instr'n Buffer/ Cache
ETLB &Tags
Data Buffer/ Cache
High Bandwidth Interfaces
Nyquist Sampled I/O
Standard Memory and I/O
audio
video
radio
net
tape
disk
PCI
DRAM

Figure 8(a)

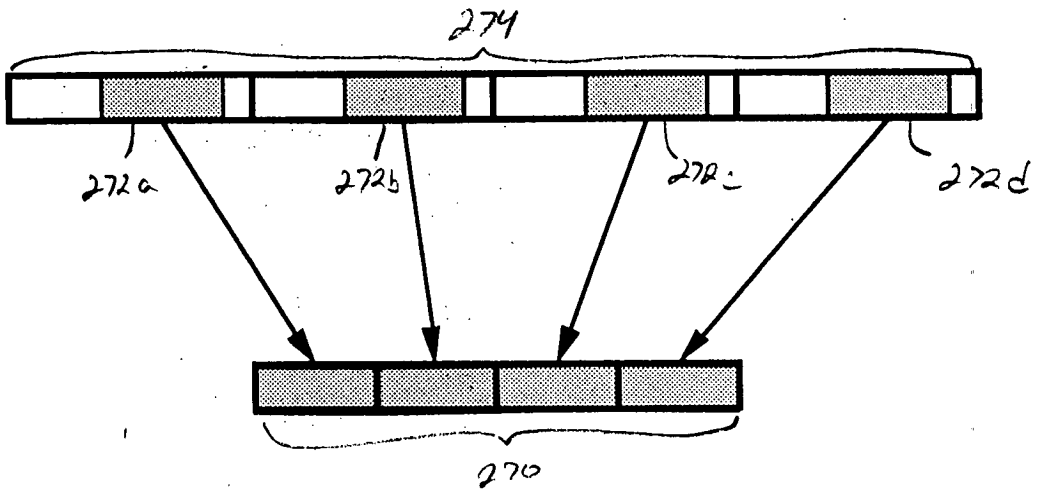
Group Expand



08/754,429

Figure 8(b)

Group Compress, Extract

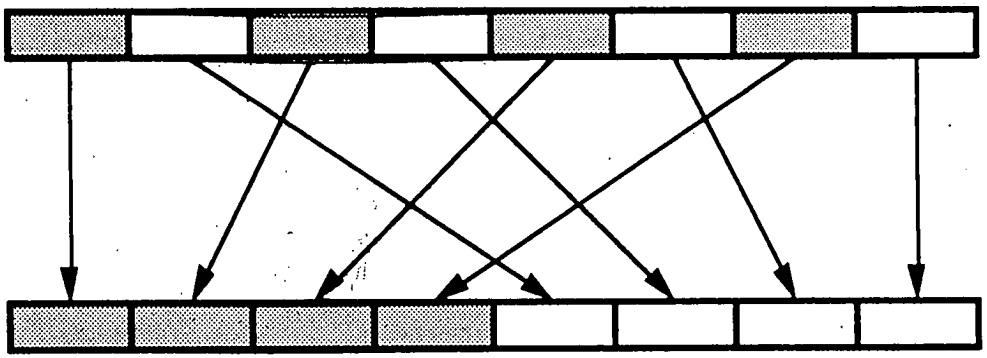


08/254,429

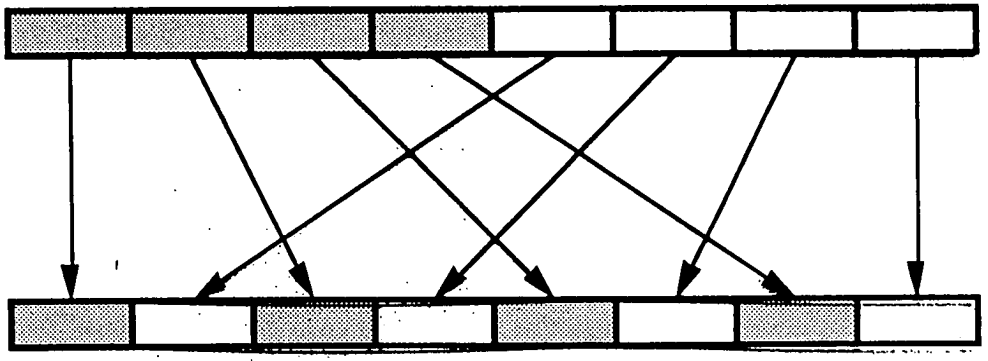
Figure 8(c)

Group Deal, Shuffle

- Group Deal: 128 bits to 128 bits



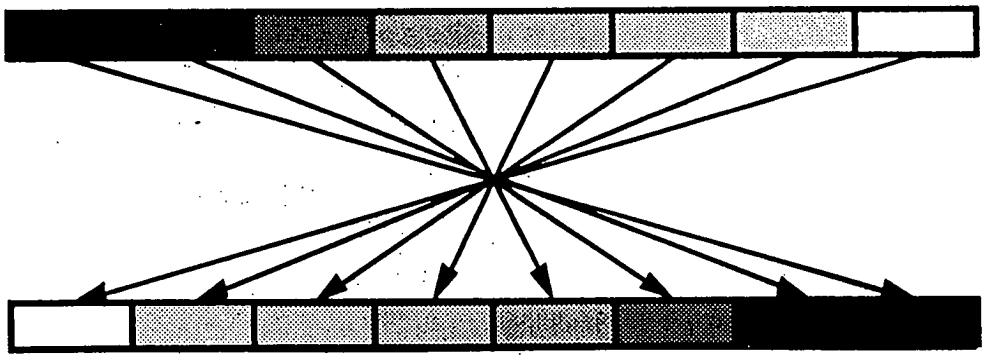
- Group Shuffle: 128 bits to 128 bits



Sony 1997

Figure 8(d)

Group Swizzle (Copy-Swap)

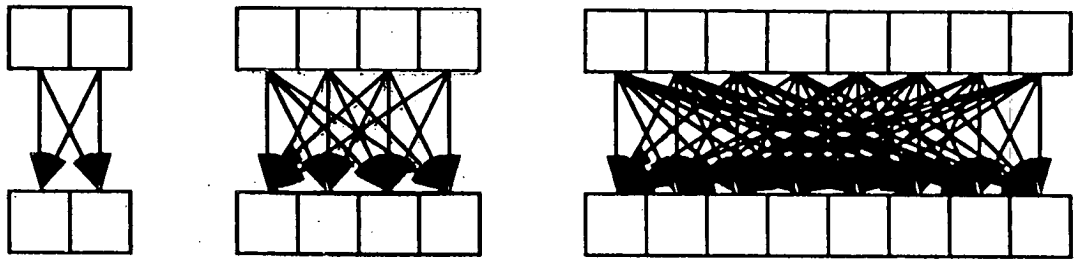


08/754,829

Figure 8(e)

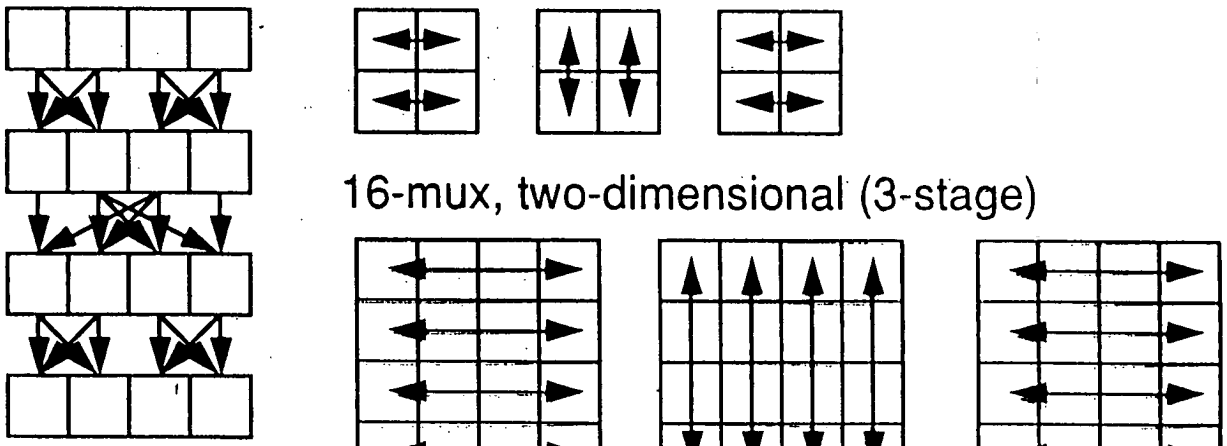
Group Permute

2-mux 4-mux 8-mux

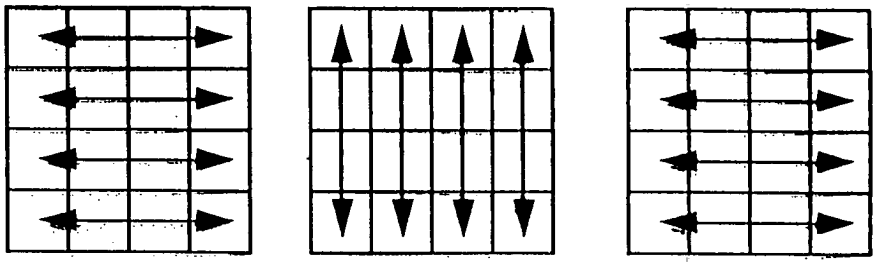


Benes network: multistage permutation

4-mux, 3 stage 4-mux, two-dimensional (3-stage)



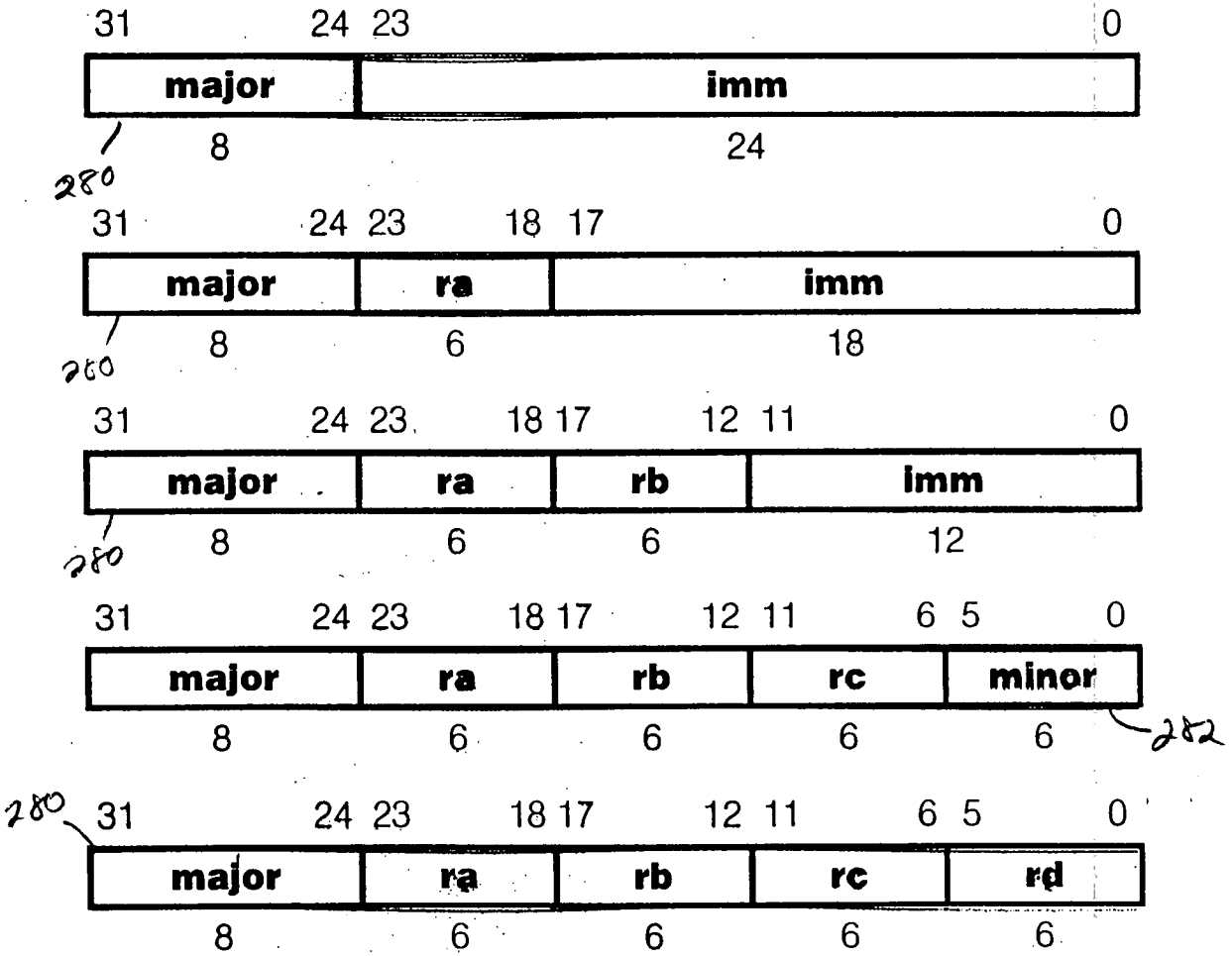
16-mux, two-dimensional (3-stage)



6,125,432 /1980

Figure 9(a)

Instruction Formats



08/754,129

Figure 9(b)

Floating-point Data Sizes

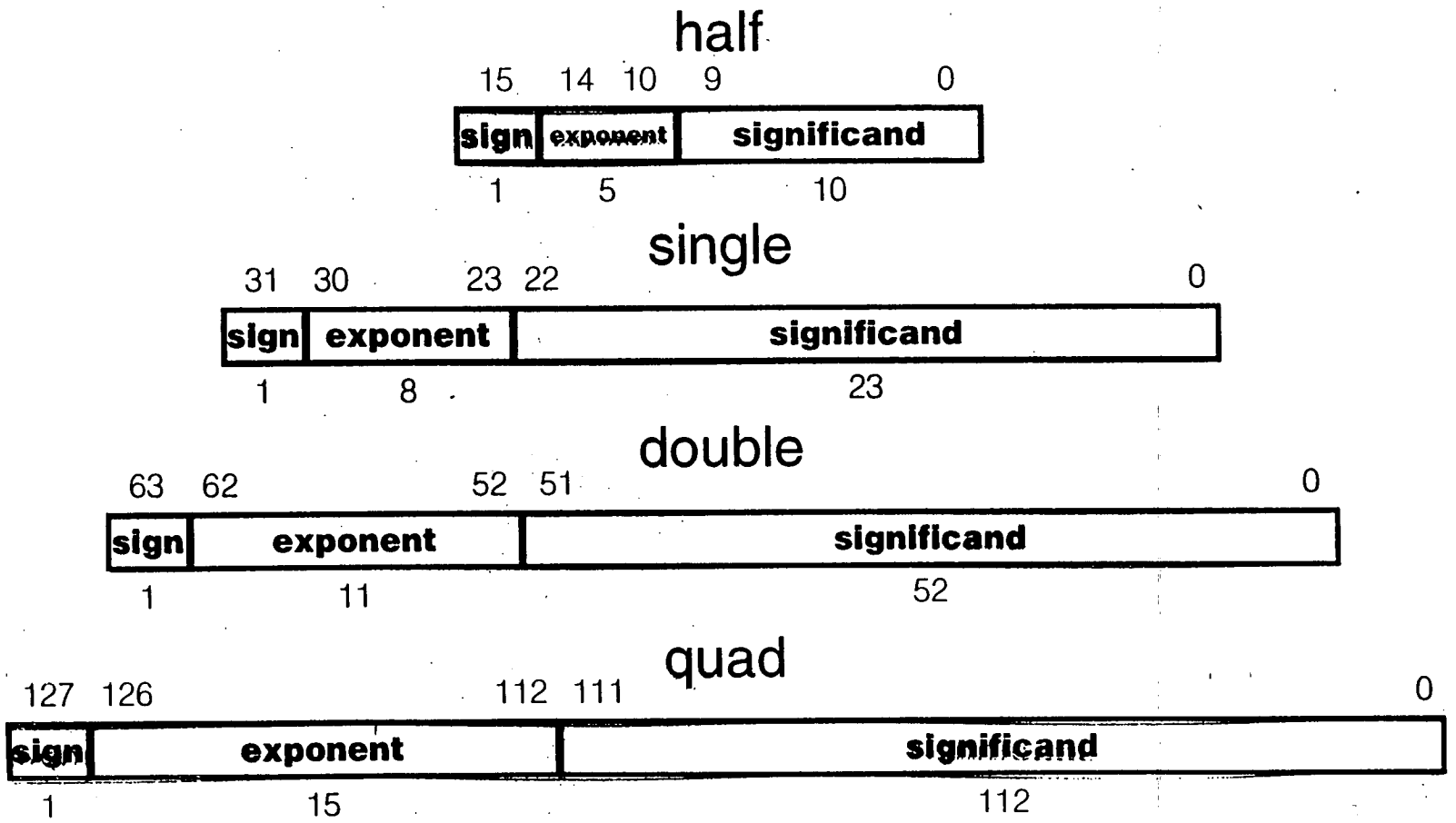
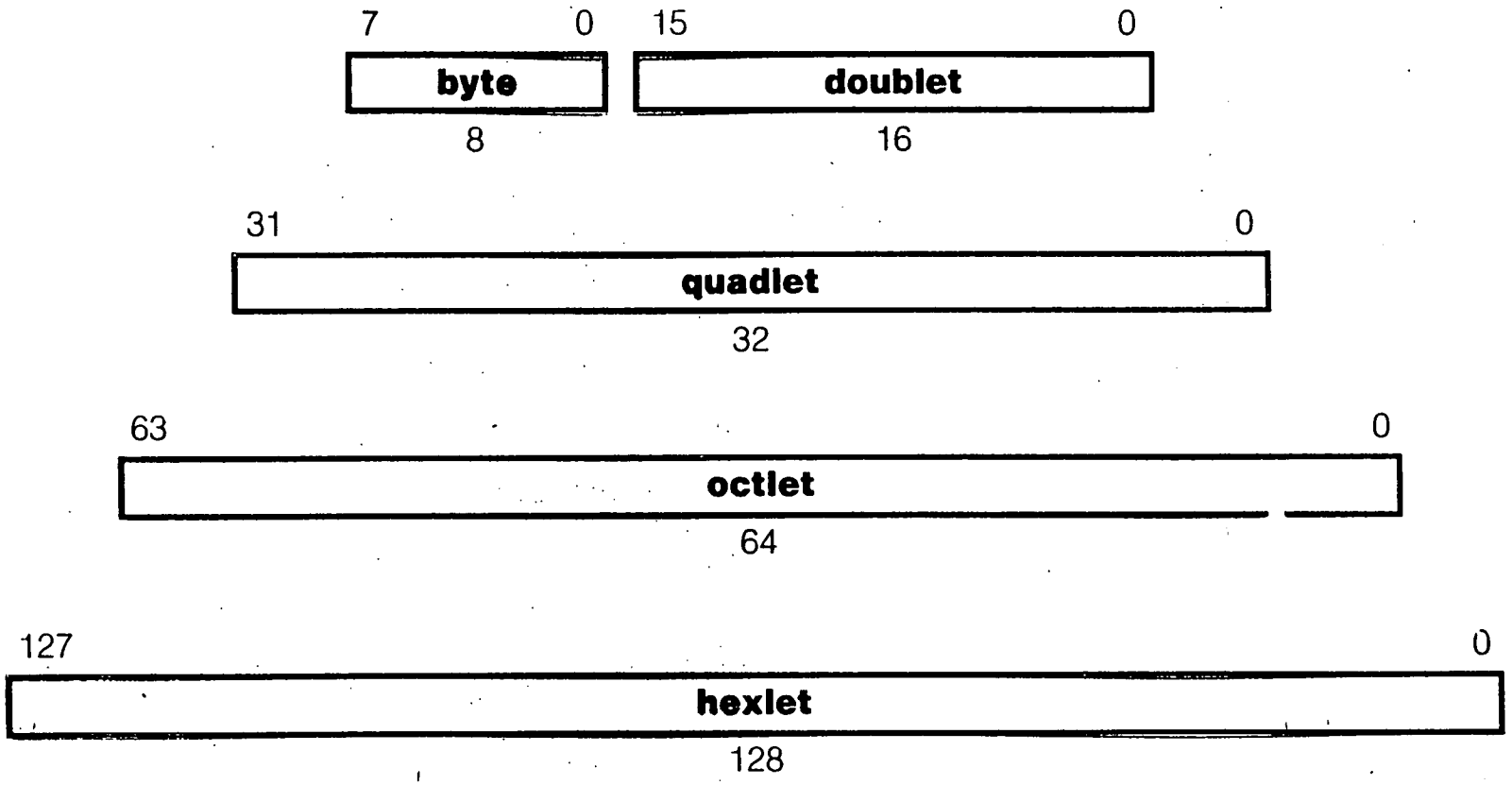


Figure 9(c)

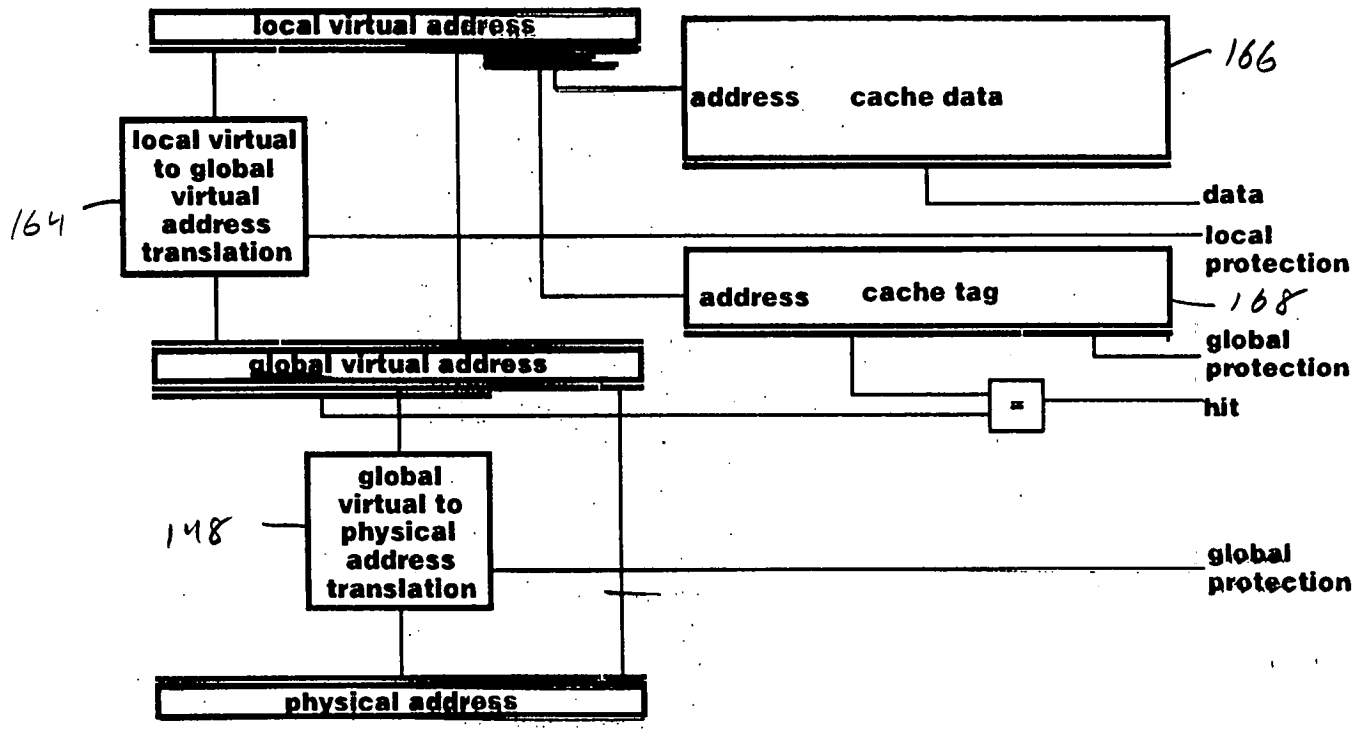
Fixed-Point Data Sizes



08/154,429

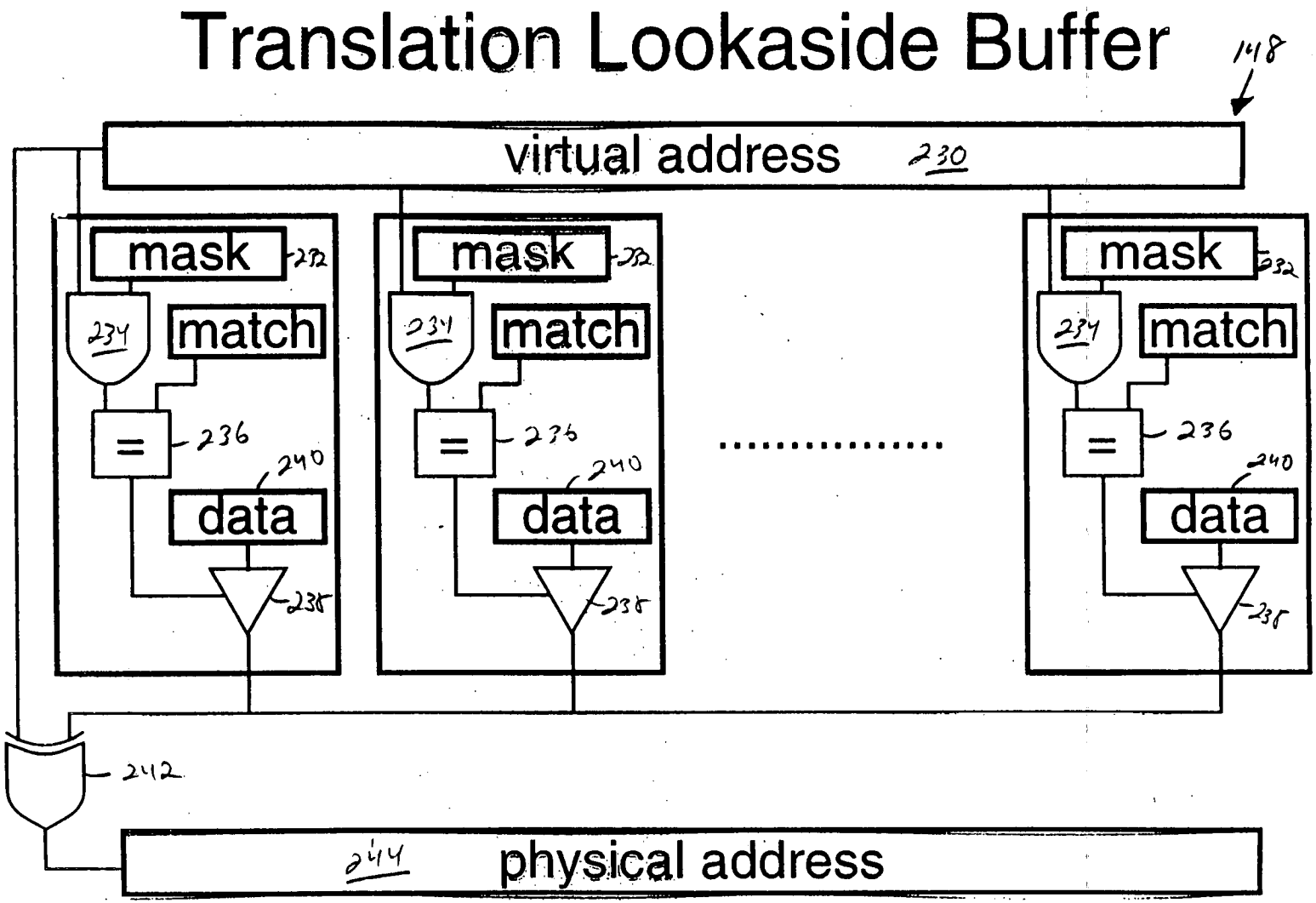
Figure 10(a)

Translation Block Diagram



6217,980

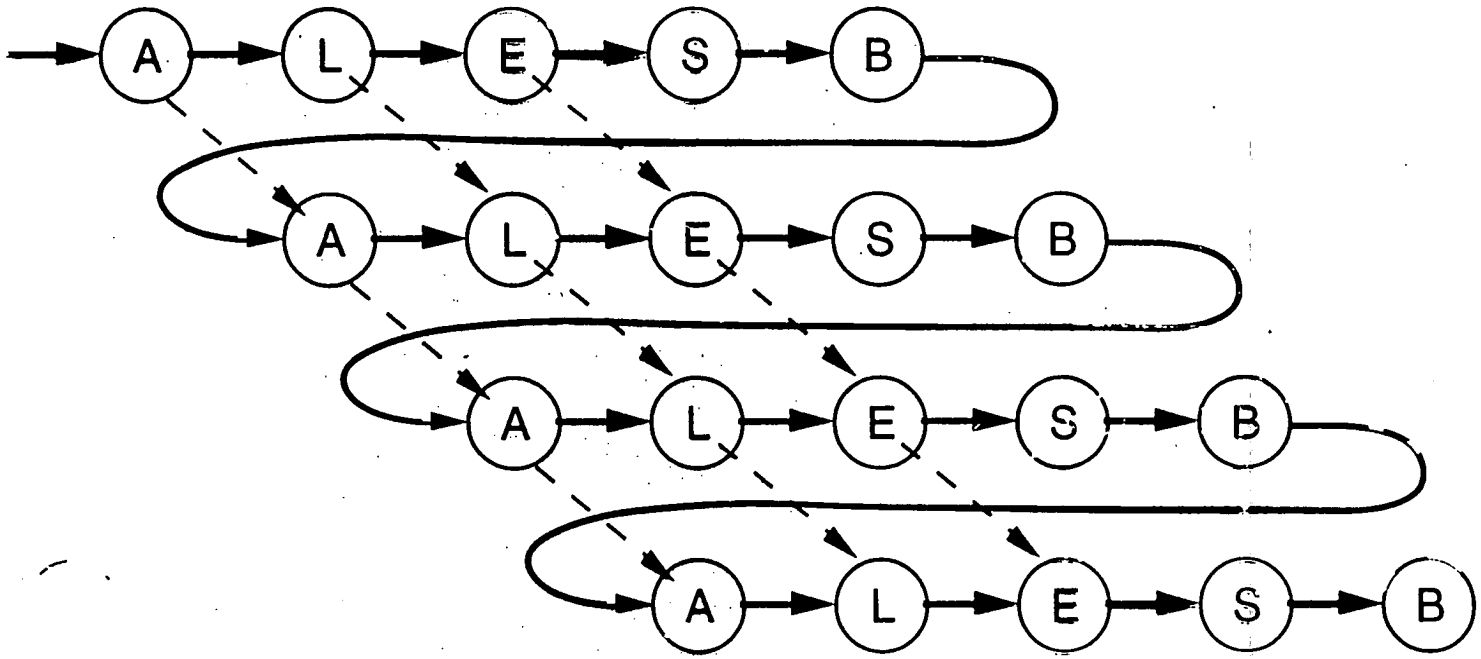
Figure 10(b)



08/054,999

Figure 11

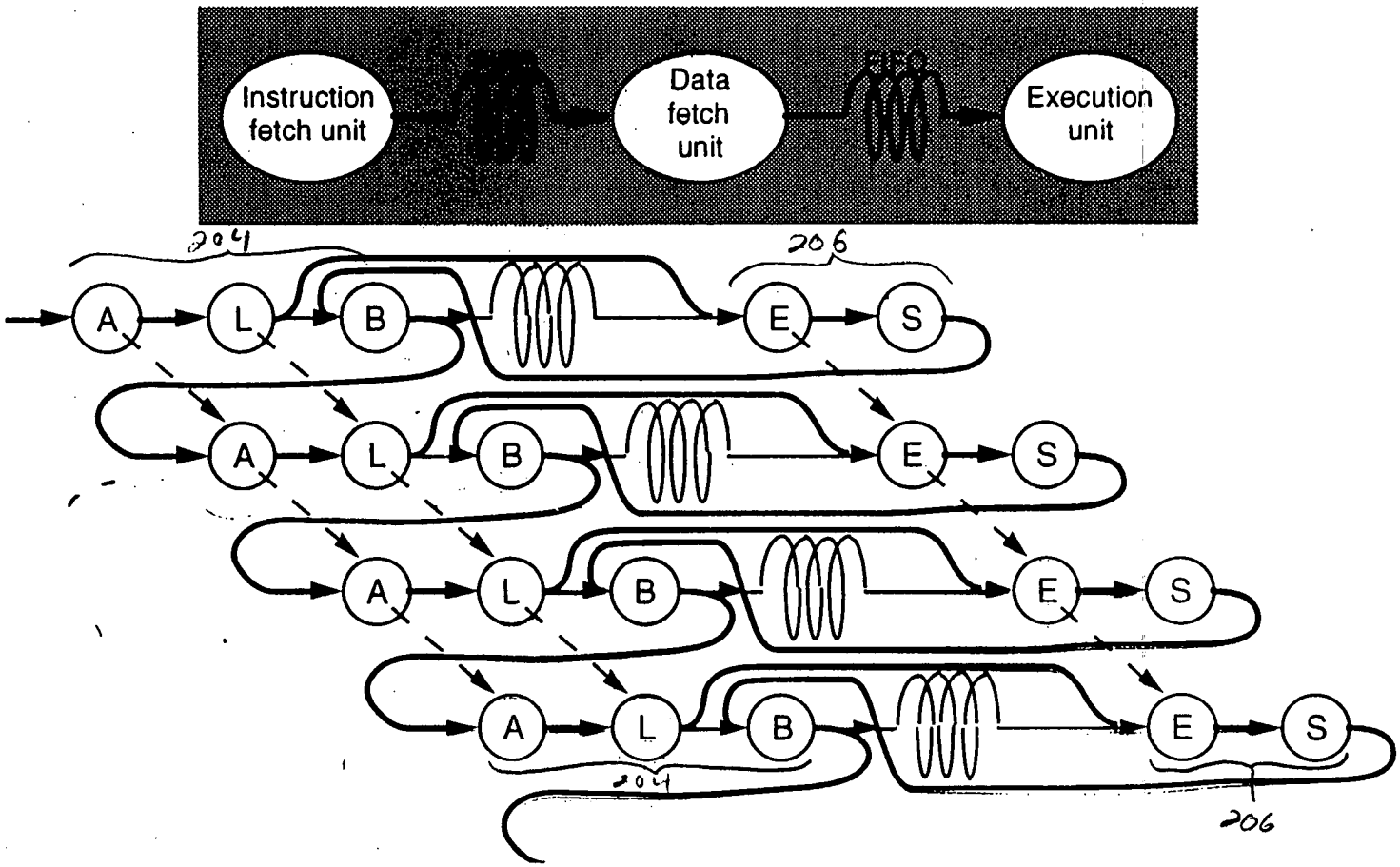
Superstring Pipeline



08/754,429

Figure 12

Superspring Pipeline



08/154429

Figure 13

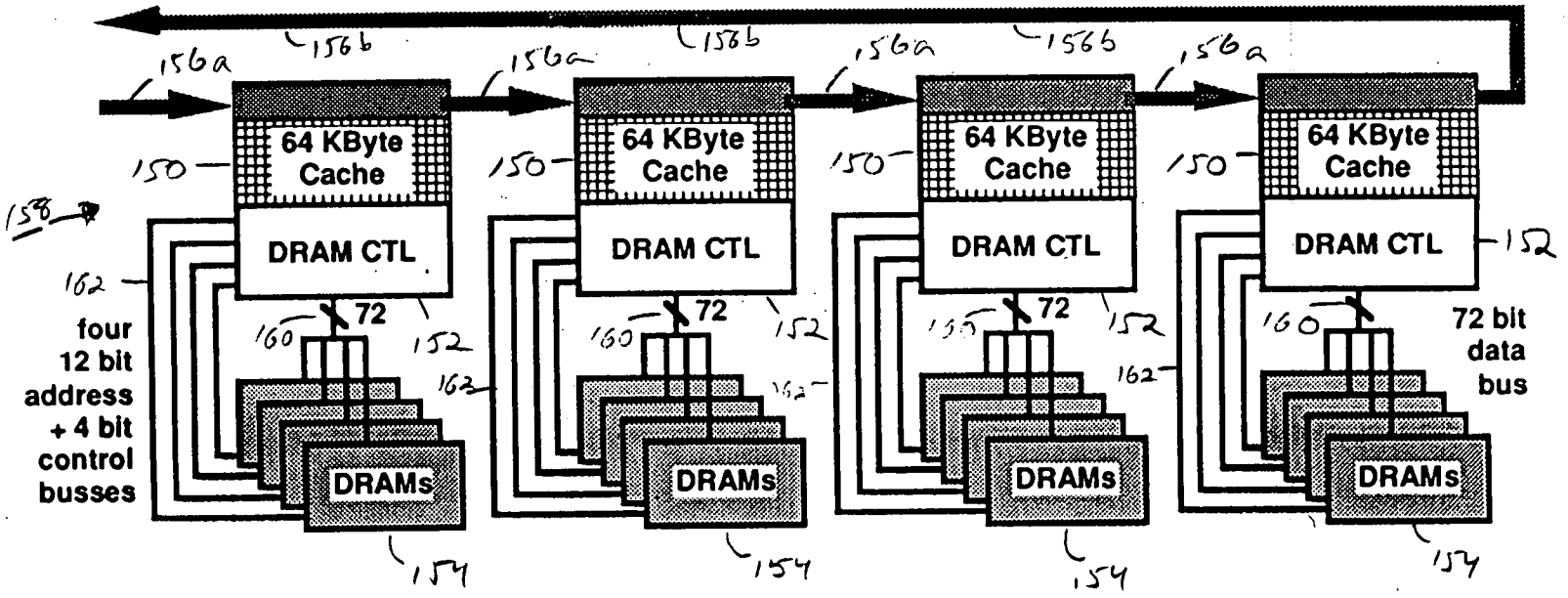

156a
156b
64 KByte Cache
150
DRAM CTL
152
158
162
four 12 bit address + 4 bit control busses
72
160
DRAMs
154
72 bit data bus

Figure 14

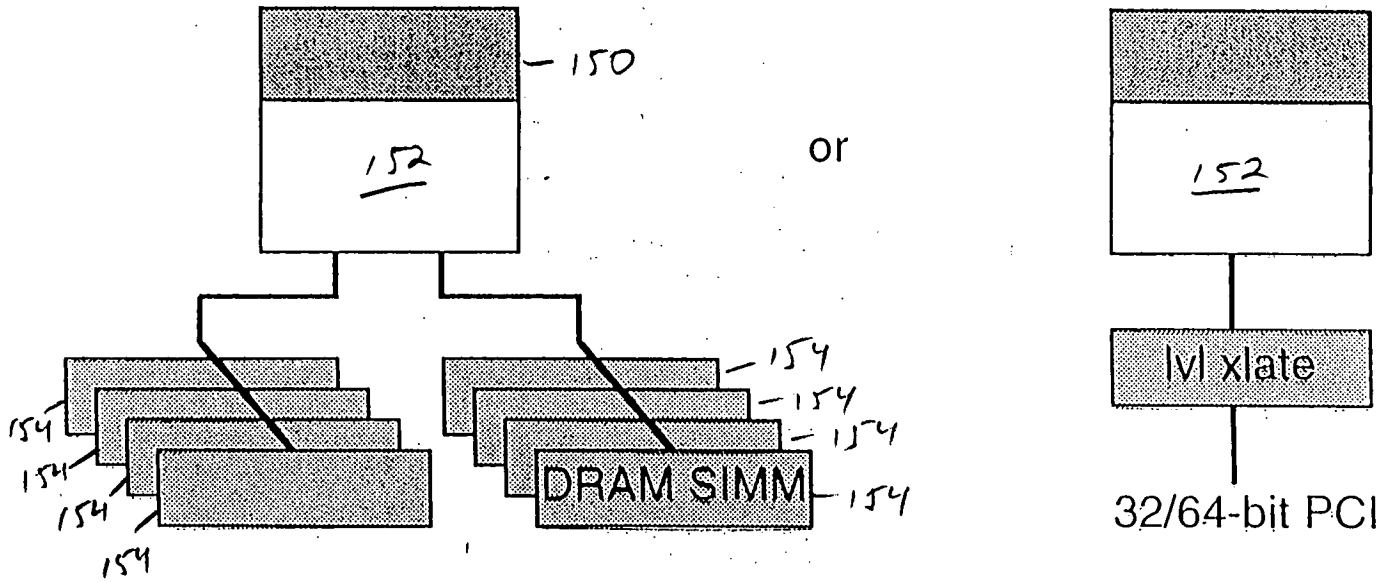
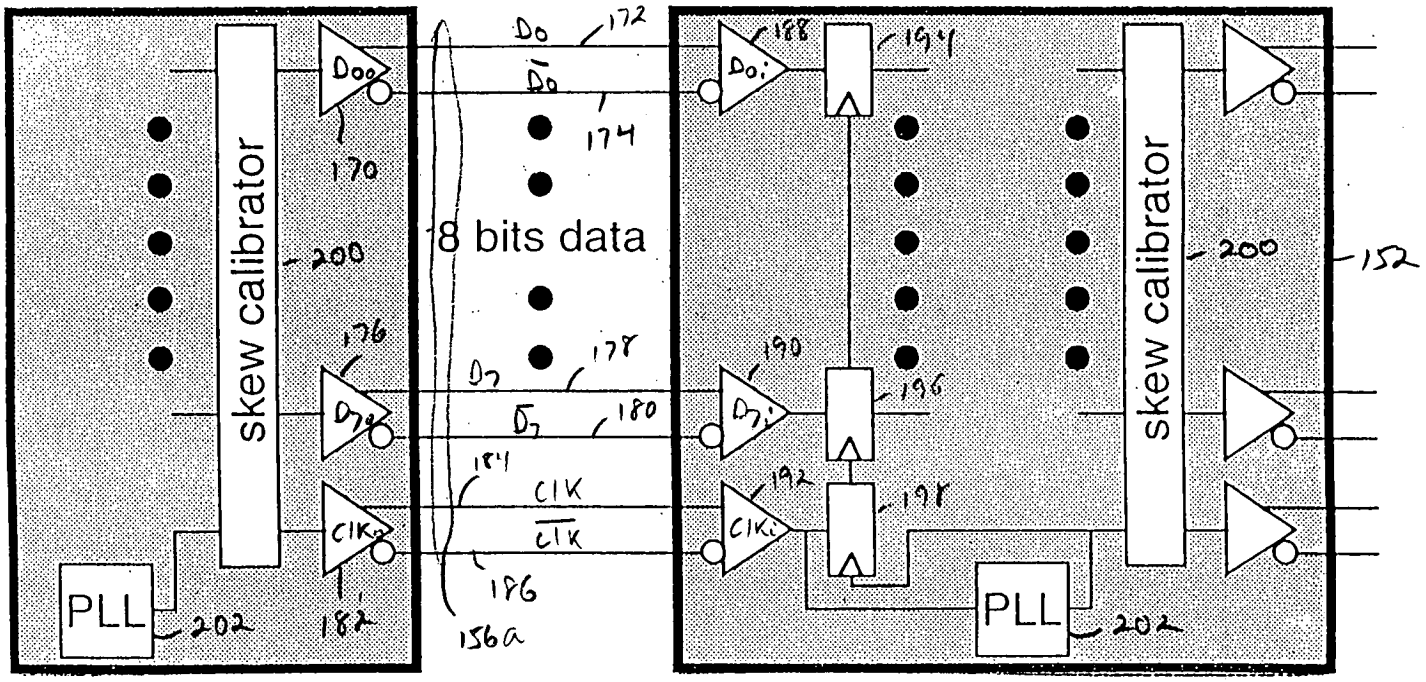
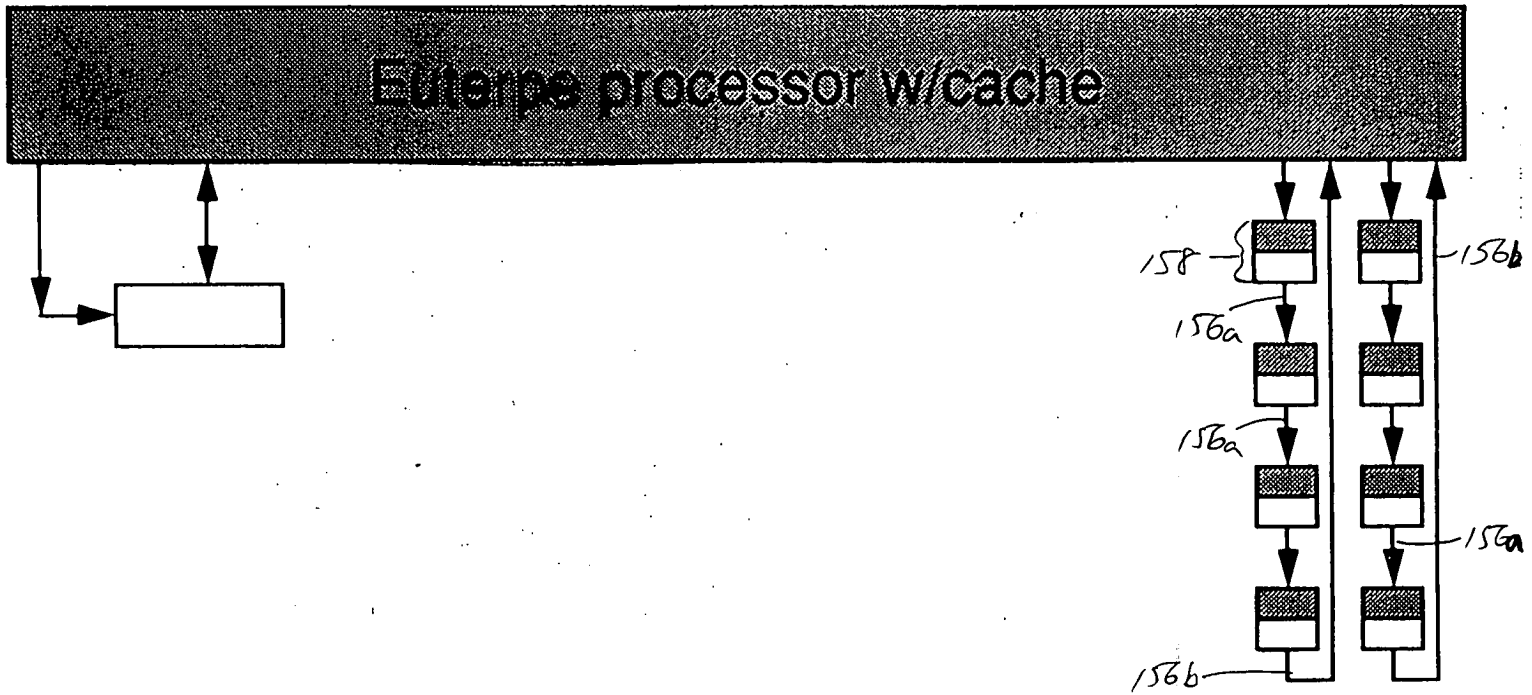

150
152
154
154
154
154
154
154
154
DRAM SIMM
or
152
lvl xlate
32/64-bit PCI

Figure 15



08/154,420

Figure 16(a)



09/254,429 12/27/99

Figure 16(b)

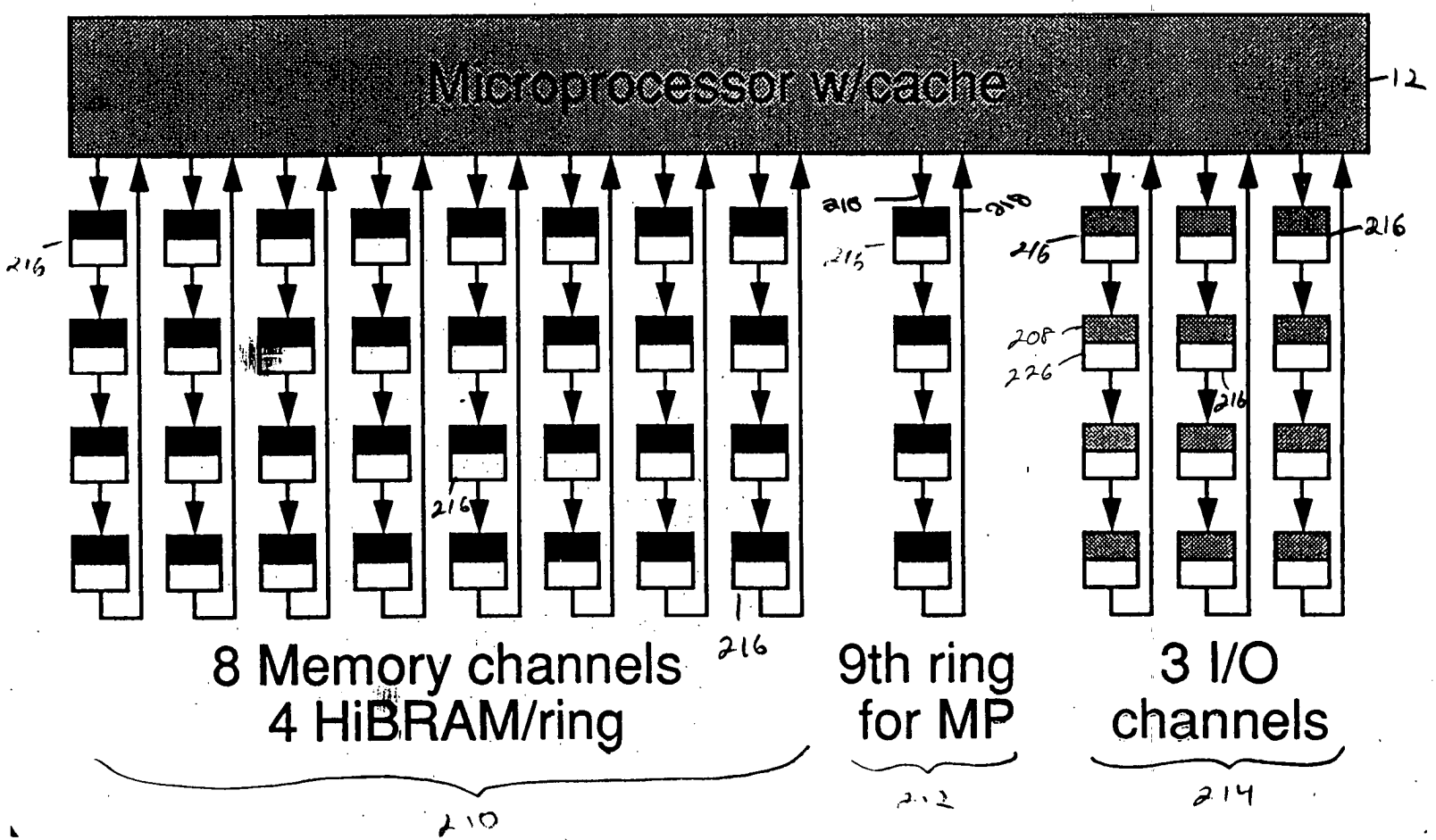
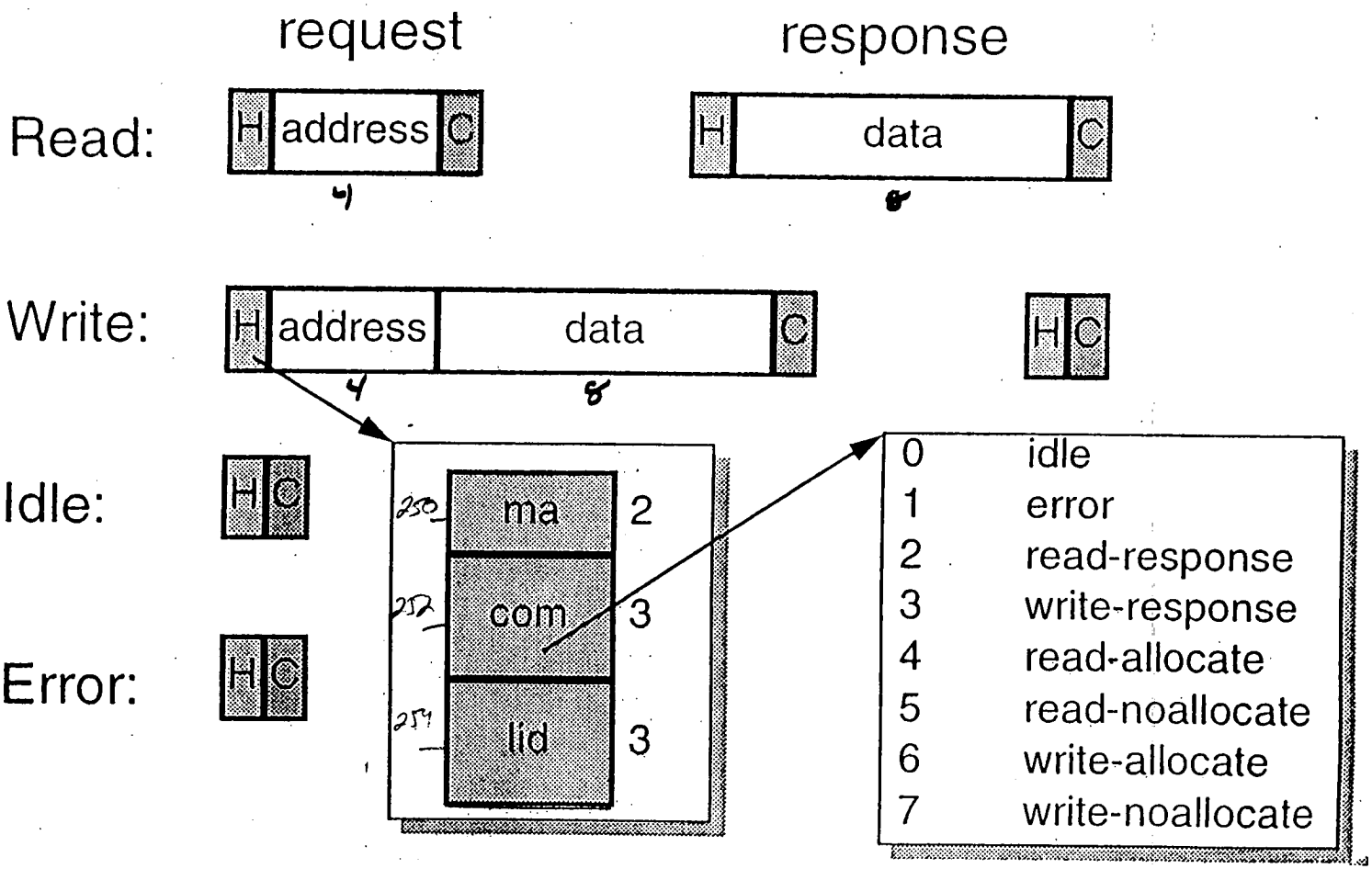
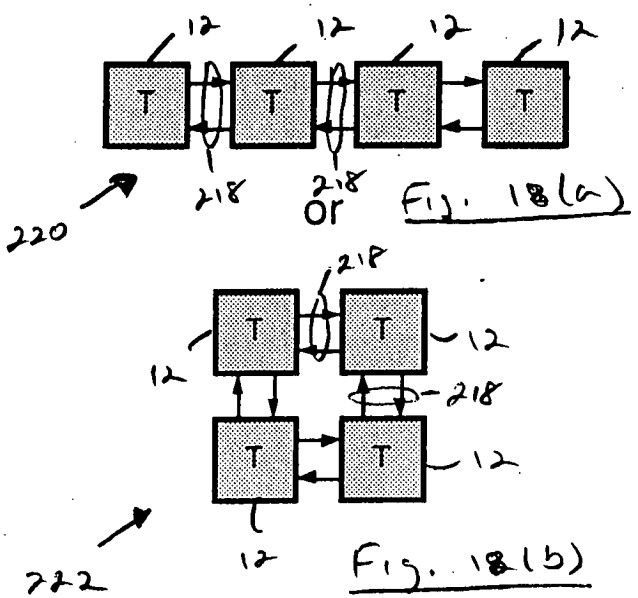

Microprocessor w/cache
12
216
210
212
208
226
8 Memory channels
4 HiBRAM/ring
9th ring
for MP
3 I/O
channels
210
212
214

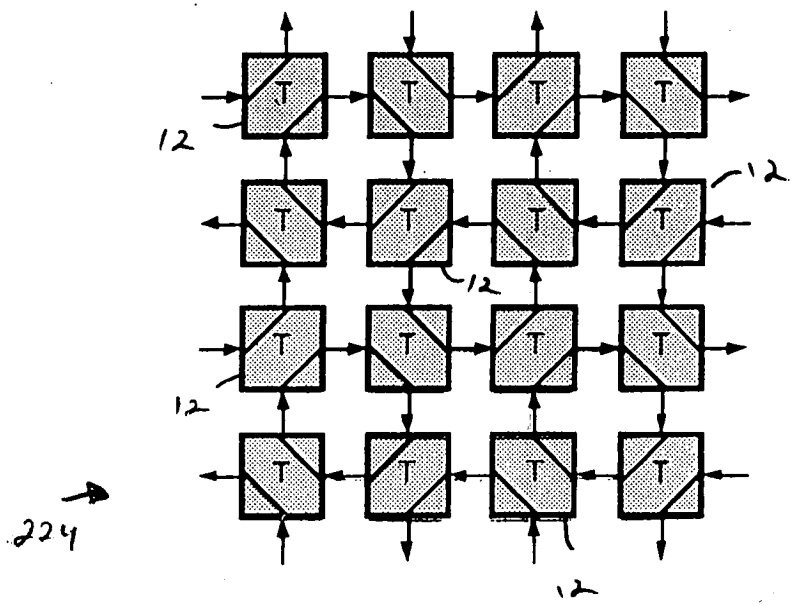
Figure 17



08/154,429

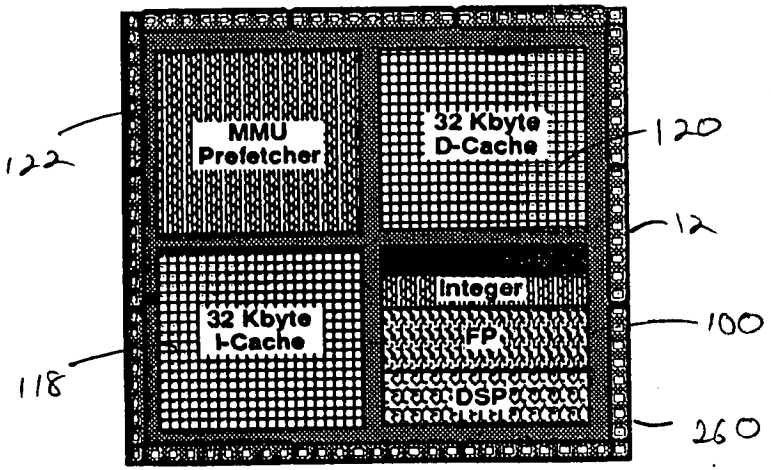
Figure 18



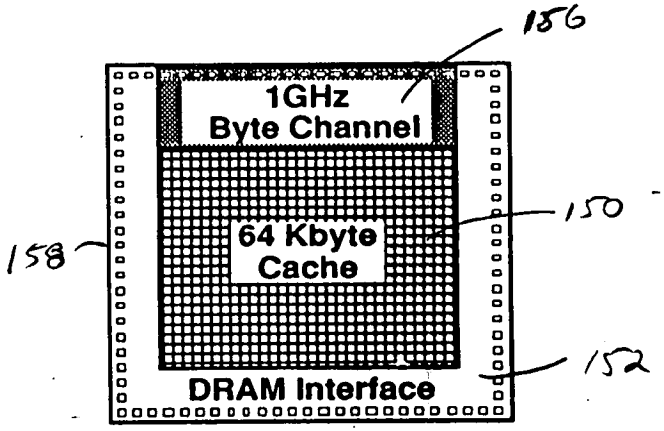


08/754,200

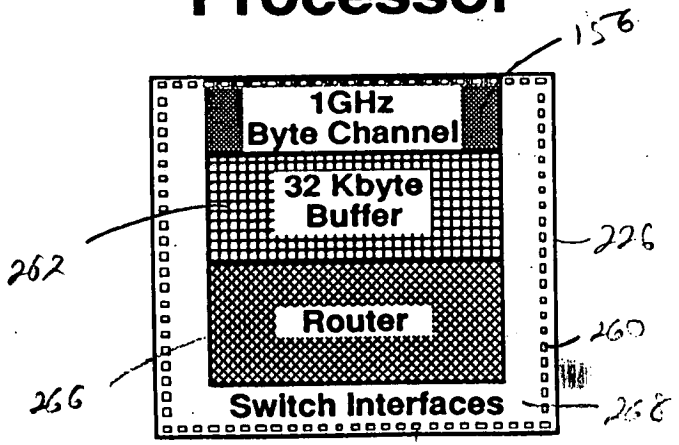
Figure 19



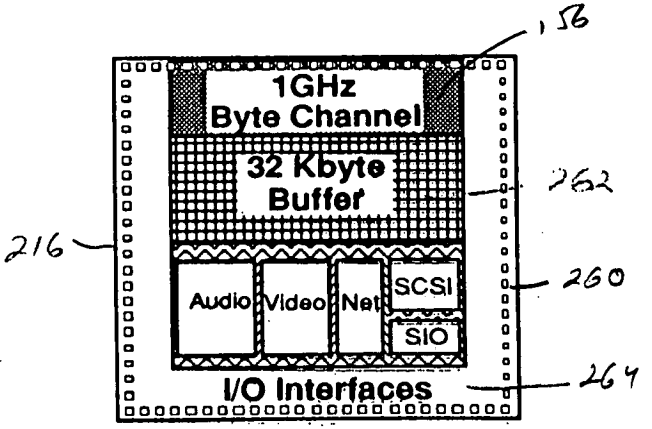
Processor



Memory



Switch



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